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EXAMINER	
BAKER, STEPHEN M	
ART UNIT	PAPER NUMBER
2133	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/15/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/784,484	RUDOSKY ET AL.	
	Examiner	Art Unit	
	Stephen M. Baker	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 July 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-42* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6,9 and 11-42* is/are rejected.

7)☒ Claim(s) *7,8 and 10* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 February 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *021804*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. Figure 3 apparently should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. Fig. 3 is apparently described in paragraph 38 as a "tree representing allowable state transitions" of a conventional convolutional code encoder", and is thus presented as an abstract diagram of encoder behavior. As abstract diagram, Fig. 3 does not appear to uniquely determine a particular tree-structured multi-stage cascade pipeline interconnection of ACS units collectively representing multiple trellis stages, although it appears possible that applicant may be unclearly indicating as much, however it's also noted that applicant elsewhere indicates (paragraph 44) that ACS details are not germane to the invention. Clarification is requested. See MPEP § 608.02(g).

2. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the method of claims 11, 21 and 30 must be shown or the features canceled from the claims. No new matter should be entered.

3. Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective

action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

4. The disclosure is objected to because of the following informalities:

In paragraph 03, "The Viterbi algorithm is a widely used convolutional code algorithm" apparently should be "The Viterbi algorithm is a widely used convolutional code decoding algorithm."

In paragraph 05, "The convolutional encoder may be described as a code tree" apparently should be "The convolutional encoder may be described using a code tree."

In paragraph 06, "taking advantage of the physical properties of the code generator to determine the maximum likelihood path through the tree to converge on the actual input sequence" apparently should be "exploiting the trellis structure of the code to determine the maximum likelihood path through the tree given the received sequence" or the like.

In paragraphs 06 and 07, "low cost" apparently should be "lower cost."

In paragraph 07, "the output device" apparently should be "the recovery" or the like.

In paragraph 13, the first sentence is incomplete; "rate of a Viterbi" apparently should be "rate of the Viterbi"; "overcomes hardware limitations" (and, similarly, subsequent references to "hardware operating delays associated with the decoder" in paragraphs 16 and 31) is apparently a reference to limiting the traceback memory word

size to 32-bits in the context of ACS units generating path decisions as 64-bit words, however it's not made clear.

In paragraph 20, "in accordance with" apparently should be "used with."

In paragraph 38, "illustrates a tree representing the allowable state transitions for an input data stream because convolutionally encoded data is decoded" apparently should be "illustrates a tree representing the allowable state transitions for an input data stream and convolutionally encoded data is decoded" or the like.

In paragraph 40, "Viterbi decoder is an algorithm that obtains a maximum likelihood sequence estimate (MLSE)" apparently should be "Viterbi decoder uses an algorithm that obtains a maximum likelihood sequence estimate (MLSE)."

In paragraph 42, "convolutional, or Viterbi, decoder" apparently should be "Viterbi convolutional code decoder" and "metrics represents" apparently should be "metrics represent."

In paragraph 56, "degradation, of" apparently should be "degradation of."

In paragraph 58, "And that word is then going to be shifted ..." is an incomplete sentence; "Rather than accept the fact ..." is apparently a poorly-worded sentence.

In paragraph 71, "Combinations of components or steps will also be considered as being noted, where terminology is foreseen as rendering the ability to separate or combine is unclear" is unclear.

The disclosure notes that "(w)hile the code tree is typically displayed as a trellis to highlight the bound nature of the code at 2^{k-1} ... states ... the tree structure is actually preferred for purposes of this invention."

Appropriate correction is required.

Claim Objections

5. Claims 1 and 21 are objected to because of the following informalities:

In claim 1, "decoding convolutional encoded data" apparently should be "decoding convolutionally encoded data"; "path metrics calculations" and "branch metrics calculations" is not idiomatic English and apparently should be "path metric calculations" and "branch metric calculations"; "survivor bits indicating a preferred path" apparently should be "survivor bits indicating preferred paths."

In claims 1 and 21, "means for compensating for the delay introduced by said pipeline register" is indefinite in a mention of what is subjected to being compensated is lacking, and apparently should read as "means for performing operation of the trace-back circuit with compensation for the delay introduced by said pipeline register" or the like. The recited "means for compensating" apparently refers to a means for arranging path selection bits in the manner shown by any one of Figs. 8-10, (e.g. with all the path "down" selection bits in a first word and all the path "up" selection bits in a second word) and the recited delay introduced by said pipeline register is apparently a delay necessitated by the storage of 2^{k-1} path decisions for a single trellis stage (e.g. 64 decisions) as plural singly-addressable words (e.g. as two 32-bit decision words).

Claim 21 further appears to describe drawing a tree diagram ("Generating a tree") after receiving encoded data, as the only tree shown in the drawings is an abstract diagram of encoder state transitions. The limitation apparently refers to

producing a mapping of path decisions from the ACS calculations to bit locations within words of trace-back memory, such as shown by any one of Figs. 8-10.

Appropriate correction is required.

6. Claims 18-20, 27-29 and 40-42 are objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. A "system to implement the method," a "computer to implement the method," and a "computer-readable medium" are not a method *per se*, although a method can be recited as being performed by the latter two of such means, by proper amendment. With further reference to claims 18, 27 and 40, implementing a method with a "system" *per se* is not seen as placing a limitation on the method in any event.

Applicant is required to cancel the claims, or amend the claims to place the claims in proper dependent form, or rewrite the claims in independent form.

Claim Rejections - 35 USC § 112

7. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

8. Claims 2-5 and 11-42 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claims 2-4, the recited "means" is described in a logically-inconsistent "means *is* function" form, rather than in standard means-with-function ("means plus function") form.

Claim 5 is not a proper sentence.

In claim 11, regarding line 4, the recited performance of steps a-c "for each received bit" is apparently misdescriptive, and step g in lines 17-18 is also apparently similarly incorrect; "sequentially decrementing by 2 32-bit word steps" apparently should be "sequentially decrementing an address by two 32-bit word steps."

In claim 21, "said pipeline register" lacks an antecedent basis.

In claim 30 "method for implementing a Viterbi decoder, having a pipeline register, that maintains throughput and integrity comprising the steps" apparently should be "method for implementing a Viterbi decoder having a pipeline register, that maintains throughput and integrity, comprising the steps" or the like.

Claim Rejections - 35 USC § 102

9. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

10. Claims 1, 5, 6, 21-23 and 27 are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 5,996,112 to Dabiri *et al* (hereafter "Dabiri").

Dabiri discloses arrangements for performing a traceback in a Viterbi decoder for decoding convolutionally-encoded data. A "circuit means for performing path metrics calculations" generates branch metric (211) and a "circuit means for performing branch metrics calculations" (223-224) produces path selection bits, as is conventional in

Viterbi decoding. As is conventional for traceback Viterbi decoding, path selection ("survivor") bits are stored and subjected to a trace-back operation. Dabiri's RAM (225) serves as a "survivor storage for retaining survivor bits indicating a preferred path through a tree," as a "tree" is inherent in the multistage trellis structure. In Dabiri's arrangements, a block of decisions spanning multiple trellis stages (multiple words of survivor bits) is stored in a single write operation (column 9, lines 23-31). Dabiri's Buffer (226) serves as a "pipeline register for receiving a word of survivor bits from said survivor storage." Dabiri's MUX (227), which is controlled to perform the "selecting," Select Map Unit (222), Trace-Back Register (228) and Read Control (229) logic collectively serve as a "traceback circuit for selecting a tree path and for determining a next address in said survivor storage", any survivor path naturally being a "tree path." As the two operations of "selecting" and generating a "next address" are coordinated and responsive to the Buffer (226) delay, Dabiri's arrangements provide a "means for compensating for the delay introduced by said pipeline register."

Regarding claim 6, Dabiri's Buffer (226) has a single stage.

Regarding claim 21, the coupling together of multiple ACS units in Dabiri's decoding arrangements to produce multiple trellis-stages of survivor bits is "generating a tree for ... encoded data."

Regarding claims 22 and 23, each trellis stage worth of survivor bits of the multiple stages stored in one write operation is a "partition" as is each addressable word, even and odd.

Claim Rejections - 35 USC § 103

11. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

12. Claims 2-4, 9, 24-26, 28-35 and 40-42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dabiri.

Regarding claims 2-4, 24, 30-35 and 40, Dabiri does not disclose details of how the survivor decisions bits are relatively positioned within a word to be written to the survivor store. Storing decision bits in a traceback memory such that the bits are arranged with parallel adjacencies determined by the parallel state adjacencies of the code trellis (which trellis has a "tree") structure (and hence in a corresponding physical layout of single-stage-synchronous parallel ACS units) is taken to be a natural choice that would suggest itself to the ordinarily-skilled practitioner, at least because it apparently would minimize wiring lengths joining the ACS units to the survivor memory interface.

Regarding claims 28, 29, 41 and 42, Dabiri does not disclose implementing the logical operations of the Viterbi decoding arrangements by means of software. Official Notice is taken that the usefulness of software in performing logic operations for a Viterbi decoder was well known at the time the invention was made. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to implement Dabiri's logical operations by means of software. Such an implementation

would have been obvious because usefulness of software in performing logic operations was already well known.

Regarding claims 25 and 26, Dabiri does not disclose the particular encoder parameters recited by the claims. Official Notice is taken that the particular encoder parameters recited by claims 25 and 26 were conventional at the time the invention was made. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to implement Dabiri's convolutional code decoding arrangements to work with convolutional code encoders described by the parameters recited in claims 25 and 26. Such an implementation would have been obvious because the particular encoder parameters recited by claims 25 and 26 were apparently already conventional.

Regarding claim 9, 16 states per stage is considered to be within the encoder constraint length parameters specified by Dabiri, providing two 32-bit words if four stages are stored at once.

Allowable Subject Matter

13. Claims 7, 8, 10 and 36-39 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

14. Claims 11-20 would be allowable if rewritten or amended to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action.

Conclusion

15. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stephen M. Baker whose telephone number is (571) 272-3814. The examiner can normally be reached on Monday-Friday (11:00 AM - 7:30 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Stephen M. Baker
Primary Examiner
Art Unit 2133

smb